

REMARKS

This is a full and timely response to the non-final Office Action of August 16, 2004. Reexamination, reconsideration, and allowance of the application and all presently pending claims are respectfully requested.

Upon entry of this First Response, claims 1-40 are pending in this application. Claims 1, 3, 4, and 6 are directly amended herein, and claims 26-40 are newly added. It is believed that the foregoing amendments add no new matter to the present application.

Response to Claim Rejections

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. See, *e.g.*, *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983).

Claim 1

Claim 1 presently stands rejected under 35 U.S.C. §102 as allegedly being anticipated by *Dishon* (U.S. Patent No. 4,849,978). Claim 1, as amended reads as follows:

1. A computer system capable of performing backward error recovery, comprising:
 - a memory unit having a plurality of memory locations; and
 - a memory controller configured to maintain a checksum in one of said memory locations, said memory controller further configured to receive a plurality of requests to update said checksum with a plurality of combined data values, said memory controller configured to combine said checksum to each of said combined data values and to store each of said combined data values, ***at least one of said combined data values representing a result of combining a first data value with a second data value, wherein said first data value and said second data value are stored at different times in the same memory location of a memory unit, said memory controller further configured to retrieve a plurality of said combined data values, including said one combined data value, in response to a data error and to recover a previous state of a particular memory location by combining each of said retrieved data values to said checksum.*** (Emphasis added)

Applicants respectfully assert that *Dishon* fails to disclose at least the features of claim 1 highlighted hereinabove. Accordingly, the 35 U.S.C. §102 rejection of claim 1, as amended, is improper.

In this regard, *Dishon* discloses the use of a checksum memory unit to backup data stored in other similarly configured memory units. To backup data, combined data values appear to be exclusively ored with a checksum stored in the checksum memory unit. In particular, when a new data value is stored in memory unit k at address i , the new data value is exclusively ored with the old data value stored at the same address to form a combined value, and this combined value is then exclusively ored with the associated checksum in the checksum memory unit. See column 4, line 66, through column 5, line 6. However, there is nothing to indicate that the combined data value is retrieved in response to a data error and used to recover a previous state of a particular memory location by combining the combined data value with the checksum.

Instead, to recover a lost data value, it appears that data values stored in other memory units are retrieved and exclusively ored with the checksum in order to recover a data value within a failed memory unit. See column 5, lines 7-11. There is nothing in *Dishon* to indicate that any such retrieved data value is a “combined” data value “representing a result of combining a first data value with a second data value, wherein said first data value and said second data value are stored at different times in the same memory location,” as recited by claim 1. Thus, *Dishon* fails to disclose at least the features of claim 1 highlighted hereinabove.

Accordingly, Applicants respectfully assert that claim 1 is allowable and request that the 35 U.S.C. §102 rejection of this claim be withdrawn.

Claims 2-9 and 26-33

Claims 2, 3, 8, and 9 presently stand rejected in the Office Action under 35 U.S.C. §102 as allegedly being anticipated by *Dishon*. Further, claims 4-7 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over *Dishon* in view of *Watson* (U.S. Patent No. 3,573,851), and claims 26-33 have been newly added via the amendments set forth herein. Applicants submit that the pending dependent claims 2-9 and 26-33 contain all features of their respective independent claim 1. Since claim 1 should be allowed, as argued hereinabove, pending dependent claims 2-9 and 26-33 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 10

Claim 10 presently stands rejected under 35 U.S.C. §102 as allegedly being anticipated by *Dishon*. Claim 10 presently reads as follows:

10. A computer system capable of performing backward error recovery, comprising:

a plurality of memory units, each of said memory units having a plurality of memory locations; and

a plurality of memory controllers configured to store to and retrieve from said memory units, one of said memory controllers configured to maintain, in a checksum memory location, a checksum of a checksum set, the other of said memory controllers configured to receive a plurality of write requests for writing to said checksum set, ***said other memory controllers, for each of said write requests, configured to store a first data value in one of said memory locations, to retrieve a second data value from said one memory location, to combine said first data value with said second data value thereby forming a combined value, and to transmit said combined value to said one memory controller,***

wherein said one memory controller is configured to update said checksum memory location with a plurality of combined values formed by said other memory controllers and to store each of said plurality of combined values, ***said one memory controller further configured to retrieve said stored plurality of combined values in response to a data error and to combine said retrieved combined values with said checksum.*** (Emphasis Added).

As set forth hereinabove in the arguments for allowance of claim 1, *Dishon* appears to disclose the use of a checksum memory unit, and data values in other memory units are retrieved and exclusively ored with a checksum in the checksum memory unit in order to recover a lost data value. See column 5, lines 7-11. However, *Dishon* fails to disclose that any such retrieved data value is a “combined” data value, as recited by pending claim 10. Accordingly, Applicants submit that *Dishon* fails to disclose each feature of claim 10, and the 35 U.S.C. §102 rejection of this claim should be withdrawn.

Claims 11-15 and 34

Claims 12 and 13 presently stand rejected in the Office Action under 35 U.S.C. §102 as allegedly being anticipated by *Dishon*. Further, claims 11, 14, and 15 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over *Dishon* in view of *Watson*, and claim 34 has been newly added via the amendments set forth herein. Applicants submit that the pending dependent claims 11-15 and 34 contain all features of their respective independent claim 10. Since claim 10 should be allowed, as argued hereinabove, pending dependent claims 11-15 and 34 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 16

Claim 16 presently stands rejected under 35 U.S.C. §102 as allegedly being anticipated by *Dishon*. Claim 16 presently reads as follows:

16. A method for performing backward error recovery, comprising the steps of:
storing a plurality of data values within a checksum set to a plurality of memory locations, said checksum set including a checksum value and a plurality of non-checksum values;
updating one of said memory locations with a first value;
combining said first value to a second value to form a combined value, said second value stored in said one memory location prior to said updating step;
updating said checksum value with said combined value;
storing said combined value;
retrieving said combined value in response to a data error;
combining said value retrieved in said retrieving step to said checksum value; and
recovering a previous state of said one memory location based on said combining said retrieved value step. (Emphasis added).

As set forth hereinabove in the arguments for allowance of claim 1, *Dishon* appears to disclose the use of a checksum memory unit, and data values in other memory units are retrieved and exclusively ored with a checksum in the checksum memory unit in order to recover a lost data value. See column 5, lines 7-11. However, *Dishon* fails to disclose that any such retrieved data value is a “combined” data value, as recited by pending claim 16. Accordingly, Applicants submit that *Dishon* fails to disclose each feature of claim 16, and the 35 U.S.C. §102 rejection of this claim should be withdrawn.

Claims 17-20

Claim 17 presently stands rejected in the Office Action under 35 U.S.C. §102 as allegedly being anticipated by *Dishon*. Further, claims 18-20 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over *Dishon* in view of *Watson*. Applicants submit that the pending dependent claims 17-20 contain all features of their respective independent claim 16. Since claim 16 should be allowed, as argued hereinabove,

pending dependent claims 17-20 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 21

Claim 21 presently stands rejected under 35 U.S.C. §102 as allegedly being anticipated by *Dishon*. Claim 21 presently reads as follows:

21. A method for performing backward error recovery, comprising the steps of:

- storing a plurality of data values within a checksum set to a plurality of memory locations, said checksum set including a checksum value and a plurality of non-checksum values;
- assigning said memory locations to different protection domains;
- storing new non-checksum values to said memory locations;
- for each of said new non-checksum values stored to one of said memory locations, combining said new non-checksum value with a value previously stored in said one memory location thereby forming a combined value;***
- updating said checksum value with each combined value formed via said combining step;
- storing into memory each combined value formed via said combining step;
- detecting a data error;
- identifying a protection domain associated with said data error;
- selecting a plurality of combined values formed in said combining step*** based on said identifying step;
- combining each of said selected combined values with said checksum value in response to said data error;*** and
- recovering a previous state of one of said memory locations based on said combining each of said selected combined values step.*** (Emphasis added).

As set forth hereinabove in the arguments for allowance of claim 1, *Dishon* appears to disclose the use of a checksum memory unit, and data values in other memory units are retrieved and exclusively ored with a checksum in the checksum memory unit in order to recover a lost data value. See column 5, lines 7-11. However, *Dishon* fails to disclose that any such retrieved data value is a “combined” data value, as recited by pending claim 21. Accordingly, Applicants

submit that *Dishon* fails to disclose each feature of claim 21, and the 35 U.S.C. §102 rejection of this claim should be withdrawn.

Claims 22-25

Claims 22-25 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over *Dishon* in view of *Watson*. Applicants submit that the pending dependent claims 22-25 contain all features of their respective independent claim 21. Since claim 21 should be allowed, as argued hereinabove, pending dependent claims 22-25 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 35

Claim 35 has been newly added via the amendments set forth herein. Claim 35 presently reads as follows:

35. A method for performing backward error recovery, comprising the steps of:
maintaining a checksum;
storing a first data value in a memory location;
storing a second data value in said memory location in response to a write request;
combining said first data value and said second data value to form a combined data value in response to said write request;
combining said combined data value to said checksum in response to said write request;
storing said combined data value; and
recovering a previous state of a particular memory location in response to a data error, said recovering step comprising the steps of retrieving said combined data value and combining said combined data value to said checksum in response to said data error.

Applicants respectfully assert that the cited art fails to disclose or suggest each of the above features of claim 35. Accordingly, claim 35 is allowable.

Claims 36 and 37

Claims 36 and 37 have been newly added via the amendments set forth herein. Applicants submit that the pending dependent claims 36 and 37 contain all features of their respective independent claim 35. Since claim 35 should be allowed, as argued hereinabove, pending dependent claims 36 and 37 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 38

Claim 38 has been newly added via the amendments set forth herein. Claim 38 presently reads as follows:

38. A method for performing backward error recovery, comprising the steps of:
 maintaining a checksum;
 updating said checksum with a plurality of data values in response to write requests;
 correlating said data values with a plurality of protection domains;
 detecting a data error associated with one of said protection domains;
 determining which of said data values are correlated with said one protection domain in response to said data error; and
 updating, in response to said data error, said checksum with each of said data values determined by said determining step to be correlated with said one protection domain.

Applicants respectfully assert that the cited art fails to disclose or suggest each of the above features of claim 38. Accordingly, claim 38 is allowable.

Claims 39 and 40

Claims 39 and 40 have been newly added via the amendments set forth herein. Applicants submit that the pending dependent claims 39 and 40 contain all features of their respective independent claim 38. Since claim 38 should be allowed, as argued hereinabove, pending dependent claims 39 and 40 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

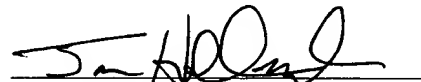
CONCLUSION

Applicants respectfully request that all outstanding objections and rejections be withdrawn and that this application and all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding Applicants' response, the Examiner is encouraged to telephone Applicants' undersigned counsel.

Respectfully submitted,

**THOMAS, KAYDEN, HORSTEMEYER
& RISLEY, L.L.P.**

By:


Jon E. Holland
Reg. No. 41,077
(256) 704-3900 Ext. 103

Hewlett-Packard Development Company, L.P.
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400